IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

Appl. No. : 10/667,019
Applicant(s): Michael W. Vice
Filed: September 18, 2003
TC/A.U.: 2800/2817
Examiner: Khanh V. Nguyen
Atty. Docket: 10030017-1
Title: COUPLED-INDUCTANCE
DIFFERENTIAL AMPLIFIER

AMENDMENT and/or RESPONSE under 37 C.F.R. § 1.111

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action of February 9, 2007, please amend the above referenced application as follows and reconsider the application in light of the following remarks.

This paper includes (each beginning on a separate sheet):

1. **Amendments to the Claims;**
2. **Remarks/Discussion of Issues;**

1. **Amendments to the Claims**:

A listing of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Previously Presented) A differential amplifier, comprising:

a pair of transistors;

a pair of inductors that provide impedance matching for the differential amplifier and that are arranged such that the inductors have a mutual inductance that increases when the differential amplifier is in a common mode.

2. (Previously Presented) The differential amplifier of claim 1, wherein the inductors comprise a transformer.

3. (Previously Presented) The differential amplifier of claim 1, wherein the inductors are arranged to provide input impedance matching for the differential amplifier.

4. (Previously Presented) The differential amplifier of claim 1, wherein the inductors are coupled to a source terminal of each transistor.

5. (Previously Presented) The differential amplifier of claim 1, wherein the inductors are arranged to provide noise control for the differential amplifier.

6. (Previously Presented) The differential amplifier of claim 1, wherein the inductors are arranged to increase common mode rejection in the differential amplifier.

7. (Previously Presented) The differential amplifier of claim 1, further comprising a second pair of inductors that are arranged to bias the transistors.

8. (Previously Presented) The differential amplifier of claim 7, wherein the second pair of inductors are arranged to have a mutual inductance that increases when the differential amplifier is excited in the differential mode.

9. (Previously Presented) The differential amplifier of claim 8, wherein the second pair of inductors comprise a transformer.

10. (Previously Presented) The differential amplifier of claim 9, wherein the second pair of inductors are arranged to provide output impedance matching.

11-20. (Cancelled).

21. (Previously Presented) A method for providing a differential amplifier, comprising providing a pair of transistors; and arranging a pair of inductors for

impedance matching to the differential amplifier such that the inductors have a mutual inductance that increases when the differential amplifier is in a common mode.

22. (Previously Presented) The method of claim 21, wherein arranging comprises arranging the inductors for form a transformer.

23. (Previously Presented) The method of claim 21, wherein arranging comprises arranging the inductors to provide input impedance matching for the differential amplifier.

24. (Previously Presented) The method of claim 21, wherein arranging comprises coupling the inductors to a source terminal of each transistor.

25. (Previously Presented) The method of claim 21, wherein arranging comprises coupling the inductors to provide noise control for the differential amplifier.

26. (Previously Presented) The method of claim 21, wherein arranging comprises coupling the inductors to increase common mode rejection in the differential amplifier.

27. (Previously Presented) The method of claim 21, further comprising arranging a second pair of inductors that bias the transistors.

28. (Previously Presented) The method of claim 27, wherein arranging a second pair of inductors comprises arranging the second pair of inductors to have a mutual inductance that increases when the differential amplifier is excited in the differential mode.

29. (Previously Presented) The method of claim 28, wherein arranging a second pair of inductors comprises arranging the second pair of inductors to form a transformer.

30. (Previously Presented) The method of claim 29, wherein arranging a second pair of inductors comprises arranging the second pair of inductors to provide output impedance matching for the differential amplifier.

REMARKS / DISCUSSION OF ISSUES

Claims 1-10 and 21-30 are presently under consideration. Claims 1 and 21 are independent claims.

Applicants gratefully acknowledge the indication of acceptance of the drawings filed on December 22, 2006.

Rejections under 35 U.S.C. § 112, ¶ 2

The rejection of claims 1, 8, 21 and 28 under this section of the Code has been considered. Applicants respectfully disagree.

The Examiner alleges that the term "when the differential amplifier is in a common mode" is vague and indefinite. The Examiner suggests alternative language as a possible meaning of the claim.

Applicants respectfully submit that the terminology 'common mode,' which appears to be the source of the alleged indefiniteness, is well within the purview of one of ordinary skill in the art, who has had the benefit of the present disclosure. For example, as described in one embodiment of the filed application:

> "In the **common mode**, the transformer T1 is excited in **common mode** from the drains of the transistors Q1 and Q2 so that the effective inductances of the windings of the transformer T1 are reduced by the effect of mutual coupling. This reduction in inductance in the **common mode** works to short out the **common mode output** of the differential amplifier 10 and improves the **common mode rejection** of the differential amplifier 10." (Emphasis provided).

Thereby, Applicants submit that not only is this terminology clear, but also provides a different embodiment than that which is provided in claim 6.

For at least the reasons set forth above, Applicants respectfully submit that the rejection of claims 1, 8, 21 and 28 is improper and should be withdrawn.

Rejections under 35 U.S.C. § 102

Claims 1-10 and 21-30 are rejected under 35 U.S.C. § 102(a) as being anticipated by *Cassan, et al.* (IEEE Journal of Solid State Electronics, Vol. 38, No. 3, March 2003.) For at least the reasons set forth herein, Applicants respectfully submit that the rejected claims are patentable over the applied art.

At the outset, Applicants provide a copy of the germane portion of the Office Action:

> Regarding claims 1, 21, Cassan et al. (**Fig. 7**) disclose a differential amplifier comprising: a pair of transistors (Q1); a pair of mutually coupled inductors (LD) that are arranged to bias the transistors (Q1) via their drains.

By contrast, claim 1 is drawn to a differential amplifier and includes:

*"...**a pair of inductors** that provide impedance matching for the differential amplifier and **that are arranged such that the inductors have a mutual inductance that increases when the differential amplifier is in a common mode.**"*

Claim 21 is drawn to a method for providing a differential amplifier and includes:

*"...providing a pair of transistors; and **arranging a pair of inductors** for impedance matching to the differential amplifier **such that the inductors have a mutual inductance that increases when the differential amplifier is in a common mode.**"*

Applicants respectfully submit that the Office Action: 1.) has provided a rejection based on features not found in either claim 1 or claim 20; and 2.) has failed to cite with any specificity whether the highlighted portions of claims 1 and 21 are even disclosed in the applied art.

As to the former, because the claims are not accurately depicted in the Office Action, Applicants respectfully submit that a meaningful reply is not possible. As to the latter, Applicants are not afforded full and complete examination of each and every feature of the pending claims; and are left to surmise how the cited reference applies to the claims under consideration. As such, the Office Action fails to comply with a basic precept of MPEP § 706 by failing to clearly articulate a rejection and thus depriving Applicants the opportunity to provide evidence of patentability at the earliest opportunity.

Therefore, Applicants respectfully submit that because the Examiner has improperly interpreted the claims, and has failed to cite the disclosure of at least one feature of claims 1 and 21, a proper rejection has not been articulated or established and that all pending claims are patentable over the applied art to *Cassan, et al.* as a matter of law.

Applicants also respectfully submit that if a rejection under this section of the Code in view of *Cassan, et al.* is asserted in the future, any such a rejection may only be made non-final in order that Applicants be afforded the opportunity to fully and completely reply to any such rejection.

Rejections under 35 U.S.C. § 103

Claims 1-10 and 21-30 are rejected under U.S.C. § 103 (a) as being unpatentable in view of *Belot* (U.S. Patent 6,639,468) and by *Cassan, et al.* For at least the reasons set forth herein, Applicants respectfully submit that the rejected claims are patentable over the applied art.

Claim 1 is drawn to a differential amplifier and includes:

"...a pair of inductors that provide impedance matching for the differential amplifier and that ***are arranged such that the inductors have a mutual inductance that increases when the differential amplifier is in a common mode.***"

Claim 21 is drawn to a method for providing a differential amplifier and includes:

"...providing a pair of transistors; and arranging a pair of inductors for impedance matching to the differential amplifier ***such that the inductors have a mutual inductance that increases when the differential amplifier is in a common mode.***"

The Office Action asserts that the applied art to *Belot* discloses all features of claims 1 and 21, except that the inductors have mutual inductance. Notably, the Office Action asserts:

> Regarding claims 1, 21, Belot discloses the claimed invention except the inductors have mutual inductance. Belot (Fig. 2) discloses a differential amplifier comprising a pair of bipolar transistors (T1A, T1B); a pair of inductors (LAA, LAB) that provide impedance matching for the differential amplifier, column 4, lines 29-34.
>
> Cassan et al. (**Fig. 7**) disclose a differential amplifier comprising a pair of transistors (Q1, Q1), each has an inductor (Ls) coupled to its source, wherein the inductors (Ls) are magnetically coupled (Ms).

Applicants respectfully point out that the highlighted portion of claims 1 and 21 are not addressed in the reproduced portion of the Office Action. Accordingly, as asserted in the traversal of the rejection under U.S.C. § 102 (a), full and complete examination of the claims, including clear citation in the applied art of each feature of the claims has not been afforded to the Applicants. As such, the Office Action fails to comply with a basic precept of MPEP § 706 by failing to clearly articulate a rejection and thus depriving Applicants the opportunity to provide evidence of patentability at the earliest opportunity. This renders this rejection improper and all claims patentable as a matter of law.

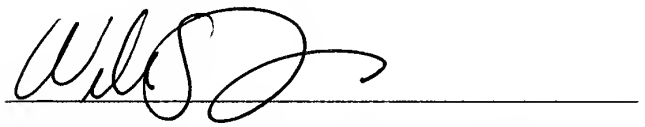
Applicants also respectfully submit that if a rejection under this section of the Code in view of *Belot* and *Cassan, et al.* is asserted in the future, any such a rejection may only be made non-final in order that Applicants be afforded the opportunity to fully and completely reply to any such rejection.

Conclusion

In view the foregoing, applicant(s) respectfully request(s) that the Examiner withdraw the objection(s) and/or rejection(s) of record, allow all the pending claims, and find the application in condition for allowance.

If any points remain in issue that may best be resolved through a personal or telephonic interview, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

Respectfully submitted on behalf of:
Avago Technologies, Inc.



by: William S. Francos (Reg. No. 38,456)
Date: June 11, 2007

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